IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method of fabricating a thin film capacitor, the method comprising ~~the steps of~~:

forming an interlayer insulating film over an entire surface of a semiconductor substrate;

forming a first via and a second via in the interlayer insulating film that ~~which~~ are spaced ~~isolated with~~ a predetermined distance from each other by selectively etching the ~~an~~ interlayer insulating film ~~formed over the entire structure of a semiconductor substrate~~;

filling in the first via and the second via with a first metal material, wherein the first metal material is planarized by chemical mechanical polishing to expose the interlayer insulating film such that the first via and the second via remain filled with the first metal material, wherein opposing surfaces of the first metal material in the first via and the second via are contacted by the interlayer insulating film;

forming a capacitor window by etching the interlayer insulating film the entire predetermined distance between the first via and the second via to have a predetermined depth such that semiconductor substrate is exposed in the capacitor window, wherein one surface of the first metal material in the first via remains in contact with the interlayer insulating film and one surface of the first metal material in the second via remains in contact with the interlayer insulating film;

forming a dielectric layer on an inner wall of the capacitor window and the exposed semiconductor substrate; and

forming a second metal material to fill in the capacitor window.

2. (Original) The method of claim 1, wherein the first via and the second via is formed by applying a photoresistive film on the interlayer insulating film and exposing and developing the photoresistive film to form a photoresistive film pattern which exposes a

portion of the interlayer insulating film where the first via and the second via having linear shape are to be formed, and then etching the exposed interlayer insulating film using the photoresistive film pattern as a mask to form the first via and the second via.

3. (Currently Amended) The method of claim 2, wherein the first via and the second via is filled with the first metal material by depositing tungsten over the entire upper surface of the interlayer insulating film including the first via and the second via to fill in the first via and the second via, and then carrying out a planarization process of chemical mechanical polishing ~~a CMP (Chemical Mechanical Polishing)~~ until the interlayer insulating film is exposed.

4. (Currently Amended) The method of claim 3, wherein the dielectric layer is formed by forming a dielectric layer on the entire upper surface of the first metal material and the interlayer insulating film and forming the second metal material on the dielectric layer to fill in the capacitor window, and then carrying out the planarization process of chemical mechanical polishing ~~a CMP~~ until the interlayer insulating film and the first material are exposed.

5. (Original) The method of claim 1, wherein the second metal material is formed of one selected from a group consisting of W, Ti, TiN, and Al.

6. (Original) The method of claim 2, wherein the second metal material is formed of one selected from a group consisting of W, Ti, TiN, and Al.

7. (Original) The method of claim 3, wherein the second metal material is formed of one selected from a group consisting of W, Ti, TiN, and Al.

8. (Original) The method of claim 4, wherein the second metal material is formed of one selected from a group consisting of W, Ti, TiN, and Al.